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Origin of the drain current bistability in polymer ferroelectric field-effect transistors

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The authors present measurements that elucidate the mechanism behind the observed drain current bistability in ferroelectric field-effect transistors based on the ferroelectric polymer poly(vinylidene fluoride-trifluoroethylene) as the gate dielectric. Capacitance-voltage measurements on metal-insulator-semiconductor diodes demonstrate that the bistability originates from switching between two states in which the ferroelectric gate dielectric is either polarized or depolarized. Pulsed charge displacement measurements on these diodes enable a direct measurement of the accumulated charge in the polarized state of 40 ± 3 mC/m^2. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2713856]

The application of the ferroelectric polymer poly(vinylidene fluoride-trifluoroethylene) [P(VDF-TrFE)] as a gate dielectric in ferroelectric field-effect transistors (FeFETs) has attracted much attention recently due to the prospect of creating a high-performance nonvolatile memory technology.[1–4] The transfer curve measurement on a FeFET in Fig. 1 illustrates the basic functionality: The ferroelectric polarization induces a large drain current bistability at zero gate bias. The semiconductor used for this measurement was the *p*-type poly(3-hexylthiophene) (P3HT) with a high hole transport mobility of 0.1 cm^2/V s.[5] Retention time measurements on this FeFET that lasted a day showed no significant drain current changes. In Fig. 1 a sharp drain current transition occurs at a gate bias of +70 V that just exceeds the ferroelectric coercive field. For this large positive gate bias, the now reversed polarization switches off the accumulation of holes, leading to a strong reduction of the drain current. However, it is not clear what happens to the polarization state of the ferroelectric after depleting the semiconductor in this way: the ferroelectric either switches into the reverse polarization keeping the semiconductor depleted, or the ferroelectric may depolarize due to the lack of free electrons in the *p*-type semiconductor that compensate for the ferroelectric polarization charge. To address such questions, we prepared P(VDF-TrFE)/P3HT based metal-insulator-semiconductor (MIS) diodes. The capacitance-voltage (*C*-*V*) scans on these diodes show that depleting the semiconductor with a positive gate bias leads to a depolarization in the ferroelectric layer. In this way, it is made clear that the polymer FeFET has a drain current bistability, because it is either in a state where the ferroelectric attracts charge carriers in the semiconductor or in a depolarized state. The drain current in the polarized on state is governed by the amount of holes accumulated in the semiconductor. The MIS diodes allow for a direct measurement of the amount of accumulated holes at the semiconductor-ferroelectric interface, confirming previous results indirectly obtained from the current response of the FeFETs.[4,5]

To fabricate the MIS diodes, we used the top-gate layout that is illustrated in the insets of Figs. 2 and 3 which enables a smooth semiconductor-insulator interface.[5] For the bottom electrodes, a chromium adhesion layer and gold were evaporated onto clean glass substrates. P3HT (electronic grade; 98.5% regioregular; Rieke Metals, Inc.) was purified as described in a previous report.[6] Filtered chloroform solutions were spin coated in a N_2 filled glovebox at 4000 rpm.[5] The 60 nm thick P3HT layers were annealed in a vacuum oven at 140 °C to enhance the crystallinity. The gate dielectric was applied by spin coating filtered 2-butanone solutions of polytrifluoroethylene (PTrFE) or P(VDF-TrFE) 65–35 mol % random copolymer (Solvay Duphar, Belgium). The samples were annealed again in a vacuum oven for 2 h at 140 °C to enhance the crystallinity of the gate dielectric. The diodes

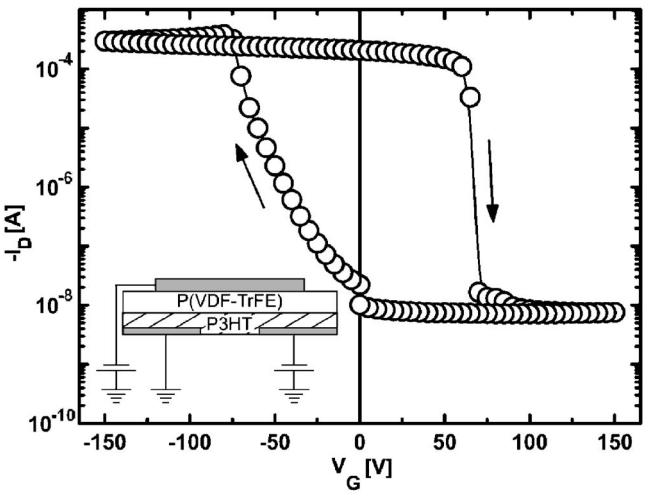

FIG. 1. Hysteretic transfer curve measurement on a top-gate FeFET with P(VDF-TrFE) as the gate dielectric and P3HT as the semiconductor. The gate-insulator layer thickness was 1.8 μm. The drain voltage V_D, channel length L, and width W are −5 V, 30 μm, and 6 mm, respectively. The data were taken from a previous report (Ref. 5). The inset presents the FeFET device layout.

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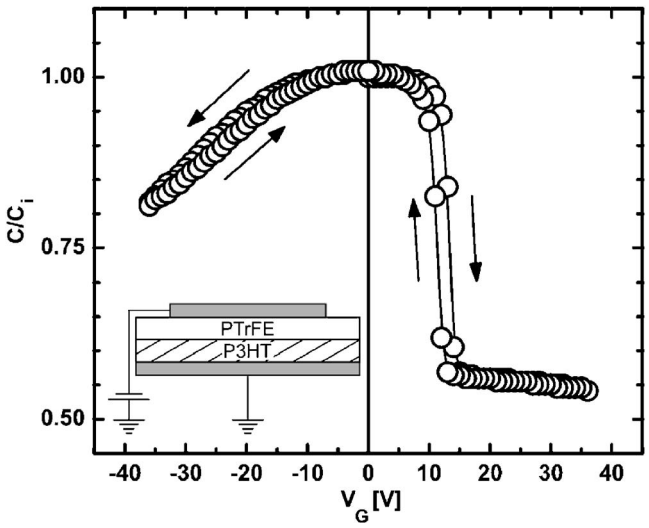

FIG. 2. Capacitance-voltage measurement on a polymer MIS diode with a nonferroelectric polytrifluorethylene gate dielectric film with a thickness of 360 nm. Capacitance C was calculated from $-\sin(\theta)/(2\pi f|Z|)$, with absolute impedance $|Z|$, phase angle θ, and ac signal frequency f. The ac signal frequency and amplitude were 1 kHz and 300 mV, respectively. The inset presents the MIS diode device layout.

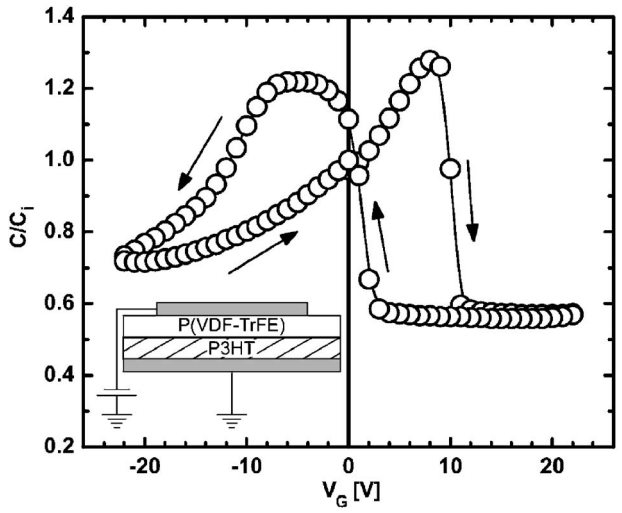

FIG. 3. Capacitance-voltage measurement on a polymer MIS diode, similar to the one presented in Fig. 2, with a 220-nm-thick ferroelectric P(VDF-TrFE) gate dielectric. The ac signal frequency and amplitude were 1 kHz and 300 mV, respectively.

were finalized by shadow mask evaporation of circular silver gate electrodes with a diameter of 1–4 mm. Measurements were performed in dark and vacuum.

As a first step, we establish the behavior of *nonferroelectric* polymer based MIS diodes with PTrFE as the gate dielectric. Since PTrFE has the same dielectric constant as the ferroelectric P(VDF-TrFE), the measurements on PTrFE based diodes serve as a reference to separate dielectric and ferroelectric effects. Figure 2 presents the typical *C-V* characteristics as measured with an Agilent 4284A *LCR* meter. In accumulation, at negative gate bias, the capacitance decreases with increasing bias. This is due to the bias-field-dependent permittivity of PTrFE, which was confirmed by *C-V* measurements on PTrFE-only capacitors. A transition towards depletion occurs at around +11 V. This positive switch-on voltage is characteristic of P3HT based FETs and is attributed to fixed charges at the semiconductor-insulator interface.[7] The depletion capacitance measured at +22 V is 0.12 nF. This is equal to the expected value derived from the reciprocal sum of the semiconductor and insulator layer capacitances C_s and C_i of 0.35 and 0.21 nF, using dielectric constant values of 3 and 11, respectively.

Having established the behavior of nonferroelectric MIS diodes, we continue in Fig. 3 with the *C-V* response of MIS diodes that have a P(VDF-TrFE) gate dielectric. In accumulation, at negative biases, the *C-V* curve has a marked nonlinearity and hysteresis. This behavior was also observed in P(VDF-TrFE)-only capacitors and stems from the bias-field-dependent permittivity of P(VDF-TrFE).[8,9] A transition towards depletion occurs at +11 V, the expected coercive voltage of the P(VDF-TrFE) layer. The depletion capacitance is again equal to the reciprocal sum of C_s and C_i. Remarkably, the scan from +22 to 0 V has a transition point at typically +4 V, where the capacitance returns to a high value. This +4 V level corresponds to the +11 V transition point in Fig. 2, considering the different gate dielectric film thicknesses. As a result, the scan from +22 to −22 V in Fig. 3 is virtually identical to the one shown in Fig. 2. This clearly shows that the ferroelectric is not remanently polarized after depleting the semiconductor. Similar observations have been done on inorganic MIS diodes.[10] If the ferroelectric would polarize, then it is not compensated by electron accumulation at the semiconductor interface. The resulting depolarization field strongly obstructs remanent ferroelectric polarization and leads to the lack of remanent depletion.[11] In the context of the recent discovery of general *n*-type behavior in organic semiconductors,[12] the present absence of electron accumulation can be explained by the use of electron-blocking semiconductor contacts. There is also a possibility of entrapment of electrons at the gate-insulator interface.[12] The results above show that the origin of bistability in our polymer FeFETs is different from most inorganic FeFETs presented in literature. Inorganic FeFETs switch between accumulation and inversion, which means that the ferroelectric polarization can be compensated in both states.

The lack of remanent depletion observed in Fig. 3 explains why Fig. 1 has a gradual drain current transition in the scan from 0 to −150 V instead of a sharp transition such as the one at +70 V. This is due to the fact that there is no sharply defined coercive field where a switching event occurs when a ferroelectric is brought from a depolarized state to a polarized state. However, we do note that our previous transfer curve measurements on FeFETs based on a poly(*p*-phenylene vinylene) (PPV) derivative semiconductor did not have the same gradual transition.[4] We attribute this observation to the different charge density dependencies of the mobility. This dependency is strongly nonlinear in the case of PPV due to a high degree of disorder.[13] With P3HT, the drain current dependence on the polarization of the gate dielectric is closer to a linear dependence, which leads to the correct observation of a gradual transition at negative gate bias in Fig. 1.

The observed depolarization behavior allows us to consider ways to optimize the memory performance of polymer FeFETs. The depolarized state in a ferroelectric is thermodynamically less stable than a polarized state.[14] Therefore, it is expected that the depolarized state will tend to return to the polarized state, which will limit the memory retention performance. To negate this effect, one can use an ambipolar semiconductor that allows for both electron and hole accu-

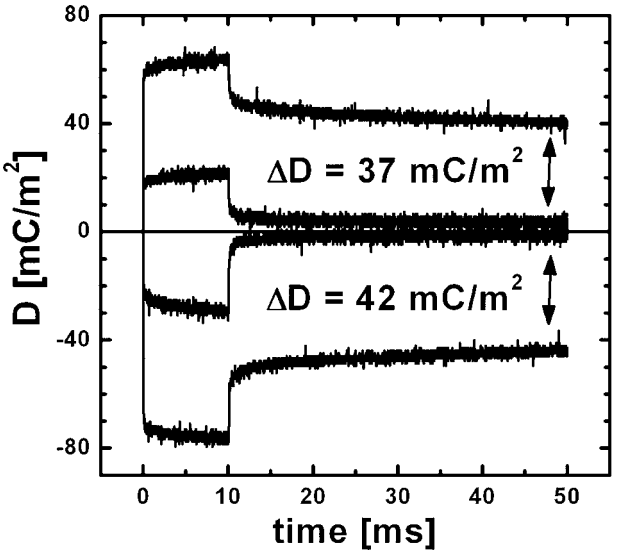

FIG. 4. Pulsed charge displacement measurements on a ferroelectric polymer MIS diode to determine the remanent charge density in the semiconductor. The P(VDF-TrFE) layer thickness was 220 nm. Voltage pulses of 10 ms and ±22 V, generated with an Agilent 8114A, were applied to the gate electrode. The charge displacement D was measured using a large capacitor connected in series with the device.

mulation. Polymer FeFETs of this type were previously demonstrated by us.[15] It is a subject of further work to see whether ambipolar FeFETs exhibit an enhanced retention.

As a final step, we quantify the amount of remanent charge that enters and leaves the MIS diodes during a programming operation, using pulsed charge displacement measurements presented in Fig. 4. This technique takes advantage of the fact that nonremanent contributions to the total charge displacement D are the same regardless of whether the ferroelectric switches or not. Subtracting the nonswitching displacement $D_{\text{non-sw}}$ from the switching displacement D_{sw} therefore gives the purely remanent displacement. The procedure for the measurement with a negative gate bias is as follows: (1) Program device with a positive gate bias; (2) short-circuit operation to remove nonremanent polarization; (3) program the device with a negative bias and measure D_{sw}; (4) short-circuit operation; and (5) program the device with a negative bias and measure $D_{\text{non-sw}}$. As shown in Fig. 4, this procedure yields a charge displacement of 40 ± 3 mC/m^2 for both a positive and a negative gate bias. The 10 ms time scale of the measurements confirms the millisecond programming time of polymer FeFETs.[4] The magnitude of the charge displacement is significantly lower than the remanent polarization of 74 mC/m^2 of P(VDF-TrFE) capacitors.[4] This is consistent with our previous attempts to measure the induced charge by comparing the current response of FETs based on P(VDF-TrFE) and PTrFE.[4,5] An observation in Fig. 4 that prompts a detailed explanation is the different $D_{\text{non-sw}}$ value for positive and negative pulses. This asymmetry arises from the fact that the semiconductor in depletion acts as an additional capacitor, which decreases the total capacitance and lowers the dielectric charge displacement.

The present results show two critical features associated with ferroelectric switching that were absent in all previous works on P(VDF-TrFE)-based MIS diodes. Firstly, the nonlinearity and hysteresis of the *C-V* curve at a negative gate bias, which are intrinsic features of P(VDF-TrFE), were absent in these previous works.[1,2,16,17] Secondly, the charge displacement measurements performed by Lim *et al.* and Gerber *et al.* yielded a negligible remanent charge displacement.[2,17] The contrasting results can be explained by the present use of an organic semiconductor instead of silicon. The latter forms a native oxide layer at the gate-insulator interface which can suppress ferroelectric switching.[11,18]

In summary, *C-V* measurements on ferroelectric polymer MIS diodes showed that a remanent depletion of charge carriers does not occur at the ferroelectric-semiconductor interface after a programming operation towards depletion. This result made it clear that polymer FeFETs have a drain current bistability, because they are either in a state where the ferroelectric attracts charge carriers in the semiconductor or in a depolarized state.

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[1] T. J. Reece, S. Ducharme, A. V. Sorokin, and M. Poulsen, Appl. Phys. Lett. **82**, 142 (2003).
[2] S. H. Lim, A. C. Rastogi, and S. B. Desu, J. Appl. Phys. **96**, 5673 (2004).
[3] K. N. N. Unni, R. de Bettignies, S. Dabos-Seignon, and J.-M. Nunzi, Appl. Phys. Lett. **85**, 1823 (2004).
[4] R. C. G. Naber, C. Tanase, P. W. M. Blom, G. H. Gelinck, A. W. Marsman, F. J. Touwslager, S. Setayesh, and D. M. de Leeuw, Nat. Mater. **4**, 243 (2005).
[5] R. C. G. Naber, M. Mulder, B. de Boer, P. W. M. Blom, and D. M. de Leeuw, Org. Electron. **7**, 132 (2006).
[6] R. C. G. Naber, B. de Boer, P. W. M. Blom, and D. M. de Leeuw, Appl. Phys. Lett. **87**, 203509 (2005).
[7] E. J. Meijer, C. Tanase, P. W. M. Blom, E. van Veenendaal, B.-H. Huisman, D. M. de Leeuw, and T. M. Klapwijk, Appl. Phys. Lett. **80**, 3838 (2002).
[8] T. Takahashi, M. Date, and E. Fukada, Appl. Phys. Lett. **37**, 791 (1980).
[9] T. Furukawa, Phase Transitions **18**, 143 (1989).
[10] P. Wurfel and I. P. Batra, Phys. Rev. B **8**, 5126 (1973).
[11] C. T. Black, C. Farrell, and T. J. Licata, Appl. Phys. Lett. **71**, 2041 (1997).
[12] L.-L. Chua, J. Zaumseil, J.-F. Chang, E. C.-W. Ou, P. K.-H. Ho, H. Sirringhaus, and R. H. Friend, Nature (London) **434**, 194 (2005).
[13] C. Tanase, P. W. M. Blom, D. M. de Leeuw, and E. J. Meijer, Phys. Status Solidi A **201**, 1236 (2004).
[14] C. Kittel, *Introduction to Solid State Physics* (Wiley, New York, 1996), p. 400.
[15] R. C. G. Naber, P. W. M. Blom, G. H. Gelinck, A. W. Marsman, and D. M. de Leeuw, Adv. Mater. (Weinheim, Ger.) **17**, 2692 (2005).
[16] K. Müller, I. Paloumpa, K. Henkel, and D. Schmeißer, Mater. Sci. Eng. C **26**, 1028 (2006).
[17] A. Gerber, H. Kohlstedt, M. Fitsilis, R. Waser, T. J. Reece, S. Ducharme, and E. Rije, J. Appl. Phys. **100**, 024110 (2006).
[18] T. P. Ma and J.-P. Han, IEEE Electron Device Lett. **23**, 386 (2002).